UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/748,219	12/27/2000	Toshio Kameshima	35.G2699	3547

5514 7590 09/10/2004

FITZPATRICK CELLA HARPER & SCINTO
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

EXAMINER	
HERNANDEZ, NELSON D	
ART UNIT	**PAPER NUMBER**
2612	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/748,219	KAMESHIMA ET AL.	
	Examiner	Art Unit	
	Nelson D. Hernandez	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27,29,35 and 36* is/are rejected.

7)☒ Claim(s) *28,30-34 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Feb 22, 2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: on line 2, the phrase "is connected" should be written as "are connected". Appropriate correction is required.

2. Claim 3 is objected to because of the following informalities: on line 3, the phrase "is connected" should be written as "are connected". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claim 27 recites the limitation "said signal reading means" in line 2. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 28 recites the limitation "said signal reading means" in line 2. There is insufficient antecedent basis for this limitation in the claim.

6. Claims 29-34 are rejected as been dependent upon rejected claims 27 and 28 under 35 U.S.C. 112.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-4 and 22-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Akimoto, US Patent 5,144,447.

Regarding claim 1, Akimoto discloses an area sensor (Fig. 2) comprising: plural pixels (Fig. 2), each having a switching element (Fig. 2: 4), arranged two-dimensionally; and plural common lines (Fig. 2: 5) which are connected to said switching elements corresponding to said pixels which are arrayed in a direction, a control signal being applied to said common line in order to drive said switching element, wherein plural driving means (Fig. 2: YDC and YDC2) for applying said control signal are connected to said common lines (Col. 4, line 67 – col. 5, line 31).

Regarding claim 2, Akimoto discloses that the driving means are connected to both ends of said common line (See fig. 2).

Regarding claim 3, Akimoto discloses that the control signal is applied at the same timing by said control means, which are connected to both ends of said common line (Col. 5, lines 9-11).

Regarding claim 4, Akimoto inherently discloses that in order to allow said plural driving means to be driven at the same time, said driving means have a start signal input section for starting the driving of said plural driving means by teaching that the common line is driven by the circuits YDC and YDC2 on the left and right sides with substantially the same clock (Col. 5, lines 9-11).

Regarding claim 22, Akimoto discloses a method of driving an area sensor (Fig. 2) having plural pixels each having a switching element (Fig. 2: 4), arranged two-

dimensionally, and having a pixel sequence in which the switching elements are connected to a common line (Fig. 2: 5), said method comprising the steps of: applying a control signal for driving said switching elements at the same time from at least two different points (Fig. 2: YDC and YDC2) of said common line; and driving the switching elements which are connected to said common line in accordance with the control signal applied to said common line (Col. 4, line 67 – col. 5, line 31).

Regarding claim 23, Akimoto inherently discloses that the control signal which is applied at the same time has the same application time period (Col. 4, line 67 – col. 5, line 31; col. 6, line 64 – col. 7, line 8).

Regarding claim 24, Akimoto discloses control signal, which is applied to said common line as applied from portions near the ends of said common line (See fig. 2).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto, US Patent 5,144,447 in view of Todaka, US Patent 4,835,617 and further in view of Petrick, US Patent 5,920,070.

Regarding claim 5, Akimoto does not explicitly disclose that the switching element is a thin-film transistor, and that the common line is a common gate line, which is connected to the gate of the thin-film transistor.

However, Todaka teaches an image pickup device wherein a common line (Fig. 3: 133) is connected to the gate of the of the switching transistors (Fig. 3: 135) and said common lines are connected to a vertical scanning circuit (Fig. 3: 111) and an auxiliary vertical scanning circuit (Fig. 3: 211) in order to effect the reading and resetting by the separate scanning circuits (Col. 4, lines 9-60; col. 7, lines 52-56).

Therefore taking the combined teaching of Akimoto in view of Todaka as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Akimoto by having a common line connected to the gate of the switching transistors and to connect said common line to a vertical scanning circuit and an auxiliary vertical scanning circuit. The motivation to do so would help the image pickup device to perform the reading and resetting by the separate scanning circuits as suggested by Todaka (Col. 7, lines 52-56).

The combination of Akimoto and Todaka does not teach that the switching element is a thin-film transistor.

However, Petrick teaches an imaging array wherein the pixel electrodes (Fig. 2A: 1) are connected to the source of thin film transistors (fig. 2: 38) (Col. 6, lines 9-25).

Therefore, taking the combined teaching of Akimoto in view of Todaka and further in view of Petrick as a whole, it would have been obvious to one of ordinary skill in the art to modify the switching transistors in Akimoto by using thin film transistors. The motivation to do so would help the sensor to reduce the size of the sensor area, reducing power consumption obtaining high-speed operation.

Regarding claim 6, the combination of Akimoto in view of Todaka and further in view of Petrick teaches that the pixel has a photoelectric conversion element, which is connected to the thin-film transistor (See Akimoto fig. 2: 1; see also Todaka, fig. 3: 113).

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Akimoto, US Patent 5,144,447 in view of Petrick, US Patent 5,920,070.

Regarding claim 7, Akimoto does not explicitly disclose that a wavelength conversion member is disposed in said pixel.

However, Petrick teaches an imaging array for X-Ray detection wherein a scintillator (Fig. 5: 35) is positioned on the photodiode to convert the X-Rays into a wavelength that the photodiode can detect (Col. 7, lines 19-25).

Therefore, taking the combined teachings of Akimoto in view Petrick as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Akimoto by incorporating a scintillator on the sensor. The motivation to do so would help the image sensor detecting the received X-Rays for performing radiography as suggested by Petrick.

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto, US Patent 4,621,291 in view of Petrick, US Patent 5,920,070.

Regarding claim 8, Takemoto discloses ~~a~~ an area sensor (Figs. 2, 5 and 7) comprising: plural pixels, each having a switching transistor (Fig. 2: 25) and a photoelectric conversion element (Fig. 2: 24), arranged two-dimensionally; and plural common source lines (Fig. 2: 26) which are connected to the source electrodes of said switching transistors which are arrayed in a direction, wherein plural signal reading

means (Fig. 2: 22A and 22B) are connected to said common source lines (Col. 2, lines 5-21; col. 4, lines 43-66). Takemoto does not explicitly disclose the switching transistors as thin film transistors.

However, Petrick teaches an imaging array wherein the pixel electrodes (Fig. 2A: 1) are connected to the source of thin film transistors (Fig. 2: 38) (Col. 6, lines 9-25).

Therefore, taking the combined teaching of Takemoto in view of Petrick as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Takemoto by using thin film transistor as a preferred switching transistor. The motivation to do so would help the sensor to reduce the size of the sensor area, reducing power consumption obtaining high-speed operation.

13. Claim 9-12, 14, 15, 18, 20 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto, US Patent 4,621,291 in view of Todaka, US Patent 4,835,617 and further in view of Petrick, US Patent 5,920,070.

Regarding claim 9, Takemoto discloses an area sensor (Figs. 2, 5 and 7) comprising: plural pixels, each having a switching transistor (Fig. 2: 25) and a photoelectric conversion element (Fig. 2: 24), arranged two-dimensionally; plural common gate lines (Fig. 2: 20) which are connected to the gate electrodes of said switching transistors which are arrayed in one direction; and plural common lines (Fig. 2: 26) which are connected to the source or drain electrodes of said switching transistors which are arrayed in another direction, wherein plural signal reading means (Fig. 2: 22A and 22B) are connected to said common lines (Col. 2, lines 5-21; col. 4,

lines 43-66). Takemoto does not teach the switching transistors as thin film transistors and that plural gate driving means are connected to the common gate lines.

However, Todaka teaches an image pickup device wherein a common line (Fig. 3: 133) is connected to the gate of the of the switching transistors (Fig. 3: 135) and said common lines are connected to a vertical scanning circuit (Fig. 3: 111) and an auxiliary vertical scanning circuit (Fig. 3: 211) in order to effect the reading and resetting by the separate scanning circuits (Col. 4, lines 9-60; col. 7, lines 52-56).

Therefore taking the combined teaching of Takemoto in view of Todaka as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Takemoto by having a common line connected to the gate of the switching transistors and to connect said common line to a vertical scanning circuit and an auxiliary vertical scanning circuit. The motivation to do so would help the image pickup device to perform the reading and resetting by the separate scanning circuits as suggested by Todaka (Col. 7, lines 52-56).

The combination of Takemoto and Todaka does not teach the switching transistors as thin film transistors.

However, Petrick teaches an imaging array wherein the pixel electrodes (Fig. 2A: 1) are connected to the source of thin film transistors (fig. 2: 38) (Col. 6, lines 9-25).

Therefore, taking the combined teaching of Takemoto in view of Todaka and further in view of Petrick as a whole, it would have been obvious to one of ordinary skill in the art to modify the switching transistors in Takemoto by using thin film transistors.

The motivation to do so would help the sensor to reduce the size of the sensor area, reducing power consumption obtaining high-speed operation.

Regarding claim 10, the combination of Takemoto in view of Todaka and further in view of Petrick teach that the signal reading means is connected to both ends of said common line (See Takemoto, figs. 2, 5 and 7).

Regarding claim 11, the combination of Takemoto in view of Todaka and further in view of Petrick teach that the gate driving means is connected to both ends of said common gate line (See Todaka, Fig. 3).

Regarding claim 12, Takemoto teaches that signal reading is performed, at the same timing, by said signal reading means, which is connected to both ends of said common line (Col. 2, lines 5-37).

Regarding claim 14, the combination of Takemoto in view of Todaka and further in view of Petrick teach the same as in claim 9. Therefore, grounds for rejecting claim 9 apply here.

Regarding claim 15, Takemoto teaches that signal reading is performed, at the same timing, by said signal reading means, which is connected to both ends of said common line (Col. 2, lines 5-37).

Regarding claim 18, the combination of Takemoto in view of Todaka and further in view of Petrick teach that the thin-film transistor comprises amorphous silicon (Col. 6, lines 9-25).

Regarding claim 20, the combination of Takemoto in view of Todaka and further in view of Petrick teach a wavelength conversion member disposed in the photoelectric conversion element (See Petrick, scintillator in fig. 5: 35; col. 7, lines 19-25).

Regarding claim 25, Takemoto discloses an image input apparatus comprising: an area sensor (Figs. 2, 5 and 7) having plural pixels arranged therein two-dimensionally, each pixel having a switching transistor (Fig. 2: 25) and a photoelectric conversion element (Fig. 2: 24), having plural common gate lines (Fig. 2: 20), which are connected to the gate electrodes of said switching transistors arrayed in one direction and plural common lines (Fig. 2: 26) which are connected to the source or drain electrodes of said switching transistors arrayed in another direction, having plural signal reading means (Fig. 2: 22A and 22B) connected to said common lines (Col. 2, lines 5-21; col. 4, lines 43-66). Takemoto does not teach having plural gate driving means connected to said common lines, and having a wavelength conversion member in the photoelectric conversion element; an electromagnetic-wave generation source; image processing means for processing an image signal from the area sensor; and display means for displaying an image on which image processing is performed; and that the switching transistors are thin-film transistors.

However, Todaka teaches an image pickup device wherein a common line (Fig. 3: 133) is connected to the gate of the of the switching transistors (Fig. 3: 135) and said common lines are connected to a vertical scanning circuit (Fig. 3: 111) and an auxiliary vertical scanning circuit (Fig. 3: 211) in order to effect the reading and resetting by the separate scanning circuits (Col. 4, lines 9-60; col. 7, lines 52-56).

Therefore taking the combined teaching of Takemoto in view of Todaka as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Takemoto by having a common line connected to the gate of the switching transistors and to connect said common line to a vertical scanning circuit and an auxiliary vertical scanning circuit. The motivation to do so would help the image pickup device to perform the reading and resetting by the separate scanning circuits as suggested by Todaka (Col. 7, lines 52-56).

The combination of Takemoto in view of Todaka does not teaches having a wavelength conversion member in the photoelectric conversion element; an electromagnetic-wave generation source; image processing means for processing an image signal from the area sensor; and display means for displaying an image on which image processing is performed; and that the switching transistors are thin-film transistors.

However, Petrick teaches an X-ray system (Fig. 1), comprising an electromagnetic-wave generation source (Figs. 1: 14 and 5: 14) wherein a scintillator (Fig. 5: 35) is positioned on the photodiode to convert the X-Rays into a wavelength that the photodiode can detect, wherein the pixel electrodes (Fig. 2A: 1) of the imaging array are connected to the source of thin film transistors (Fig. 2: 38), also teaches an image processing circuit, which coordinates the operation of the X-ray system and to provide image data (Fig. 1: 24) to the monitor (Fig. 1: 26) (Col. 5, line 64 – col. 6, line 25, col. 7, lines 19-25).

Therefore, taking the combined teaching of Takemoto in view of Todaka and further in view of Petrick as a whole, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the imaging array taught in Takemoto as claimed. The motivation to do so would provide an X-ray image sensor capable of perform real time diagnosis immediately after photographing, minimizing the waiting period of a patient.

14. Claims 13, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto, US Patent 4,621,291 and Todaka, US Patent 4,835,617 in view of Petrick, US Patent 5,920,070 and further in view of Akimoto, US Patent 5,144,447.

Regarding claim 13, the combination of Takemoto and Todaka in view of Petrick does not teach that the control signal is applied at the same timing, by said gate driving means.

However, Akimoto teaches an area sensor (Fig. 2) comprising: plural pixels (Fig. 2), each having a switching element (Fig. 2: 4), arranged two-dimensionally; and plural common lines (Fig. 2: 5) which are connected to said switching elements corresponding to said pixels which are arrayed in a direction, a control signal being applied to said common line in order to drive said switching element, wherein plural driving means (Fig. 2: YDC and YDC2) for applying said control signal at the same time are connected to said common lines (Col. 4, line 67 – col. 5, line 31).

Therefore, taking the combined teaching of Takemoto and Todaka in view of Petrick and further in view of Akimoto as a whole, it would have been obvious to one of ordinary skill in the art to apply the control signal the driving means at the same time.

The motivation to do so would be to increase the power sent to the common lines so as to turn on the transistors as suggested by Akimoto (Col. 5, lines 17-31).

Regarding claim 16, the combination of Takemoto and Todaka in view of Petrick and further in view of Akimoto teaches the same as in claim 13. Therefore, grounds for rejecting claim 13 apply here.

Regarding claim 17, the combination of Takemoto and Todaka in view of Petrick teaches that signal reading is performed, at the same timing, by said signal reading means (See Takemoto, Col. 2, lines 22-28). The combination of Takemoto and Todaka in view of Petrick does not teach that the control signal is applied at the same timing, by said gate driving means.

However, Akimoto teaches an area sensor (Fig. 2) comprising: plural pixels (Fig. 2), each having a switching element (Fig. 2: 4), arranged two-dimensionally; and plural common lines (Fig. 2: 5) which are connected to said switching elements corresponding to said pixels which are arrayed in a direction, a control signal being applied to said common line in order to drive said switching element, wherein plural driving means (Fig. 2: YDC and YDC2) for applying said control signal at the same time are connected to said common lines (Col. 4, line 67 – col. 5, line 31).

Therefore, taking the combined teaching of Takemoto and Todaka in view of Petrick and further in view of Akimoto as a whole, it would have been obvious to one of ordinary skill in the art to apply the control signal the driving means at the same time. The motivation to do so would be to increase the power sent to the common lines so as to turn on the transistors as suggested by Akimoto (Col. 5, lines 17-31).

15. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto, US Patent 4,621,291 and Todaka, US Patent 4,835,617 in view of Petrick, US Patent 5,920,070 and further in view of Mei, US Patent 6,005,238.

Regarding claim 19, the combination of Takemoto in view of Todaka and further in view of Petrick does not teach that the photoelectric conversion element comprises a material selected from the group consisting of amorphous selenium, lead (II) iodide (PbI_2) and gallium arsenide.

However, Mei teaches the use of amorphous selenium or lead iodide as an alternative material used in image sensors (Col. 5, lines 46-62).

Therefore, taking the combined teaching of Takemoto and Todaka in view of Petrick and further in view of Mei, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the material used for the photoelectric conversion element in Takemoto by using amorphous selenium or lead iodide as an alternative material. The motivation to do so would help to modify the sensor array depending on the user needs (i.e. X-Ray imaging) as suggested by Mei (Col. 5, lines 46-62).

16. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto, US Patent 4,621,291 and Todaka, US Patent 4,835,617 in view of Petrick, US Patent 5,920,070 and further in view of Kim, US Patent 6,475,824 B1.

Regarding claim 21, the combination of Takemoto and Todaka in view of Petrick does not teach that gate driving means or said signal-reading means is anisotropically connected to the common gate line or the common source line.

However, Kim teaches the use of an anisotropic bonding material (Fig. 1: 21) for connecting a drive integrated circuit chip (Fig. 1: 14) to the gate pad (Fig. 1: 12) of an X-ray detector panel (Fig. 1: 10) (Col. 1, lines 48-53; col. 5, lines 53-61).

Therefore, taking the combined teaching of Takemoto and Todaka in view of Petrick and further in view of Kim, it would have been obvious to one of ordinary skill in the art to modify Takemoto by using an anisotropic bonding material to connect the driving means to the common gate line of the sensor array. The motivation to do so would provide the image sensor with a very short connection between connecting terminals in order to reduce the connection area as suggested by Kim (Col. 1, lines 48-53).

17. Claims 26/25, 27/26 and 29/27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto, US Patent 4,621,291 and Todaka, US Patent 4,835,617 in view of Petrick, US Patent 5,920,070 and further in view of Spivey, US Patent 5,886,353.

Regarding claim 26, the combination of Takemoto and Todaka in view of Petrick does not teach a grid provided between said area sensor and said electromagnetic-wave generation source.

However, Spivey teaches an imaging device (Fig. 1), comprising an electromagnetic-wave generation source (Fig. 1: 4) and an area sensor (Fig. 1: 12), wherein an anti-scatter grid (Fig. 17B: 201) is provided between said area sensor and said electromagnetic-wave generation source (Col. 3, line 56 – col. 4, line 13; col. 14, lines 9-60; col. 15, lines 54-67).

Therefore, taking the combined teaching of Takemoto and Todaka in view of Petrick and further in view of Spivey, it would have been obvious to one of ordinary skill in the art to modify the imaging system by including an anti-scatter grid provided between the area sensor and the electromagnetic-wave generation source. The motivation to do so would help the imaging system to increase the contrast of the images received by minimizing the scattered rays from the electromagnetic-wave generation source since they do not contain usable information and may fog the images detected as suggested by Spivey (Col. 14, lines 22-36).

Regarding claim 27, the combination of Takemoto and Todaka in view of Petrick and further in view of Spivey teach that the signal reading means comprises an amplifier IC (See Petrick, fig. 3: 48 and Spivey, fig. 16: 50) having an amplifier provided individually for each data line, and an analog multiplexer and an A/D converter (See Spivey, col. 12, lines 21-42; col. 10, line 55 – col. 11, line 26; See Petrick, col. 6, line 57 – col. 7, line 4).

Regarding claim 29, the combination of Takemoto and Todaka in view of Petrick and further in view of Spivey teach that the signal reading means comprises a plurality of said amplifier ICs, and the output of each amplifier IC can be selected and controlled in accordance with a select signal (See Spivey, col. 12, lines 21-42; col. 10, line 55 – col. 11, line 26).

18. Claims 35 and 36 rejected under 35 U.S.C. 103(a) as being unpatentable over Takemoto, US Patent 4,621,291 and Todaka, US Patent 4,835,617 in view of Petrick, US Patent 5,920,070 and further in view of Waechter, US Patent 6,172,369 B1.

Regarding claim 35, the combination of Takemoto and Todaka in view of Petrick does not teach that the resistivity of the material for the common gate line is 10 μΩ•cm or more.

However, Waechter teaches a detector comprising chromium gate lines (Figs. 3: 24, 4: 24 and 5: 24)(Col. 4, line 63 – col. 5, line 2). The resistivity of chromium (Cr) is approximately 12.9 μΩ•cm.

Therefore, taking the combined teaching of Takemoto and Todaka in view of Petrick and further in view of Waechter, it would have been obvious to one of ordinary skill in the art to modify Takemoto by using chromium gate lines. The motivation to do so would help the gate lines to have high conductivity in order to increase the heat resistance of the gate lines.

Regarding claim 36, the combined teaching of Takemoto and Todaka in view of Petrick and further in view of Waechter teaches the same as in claim 35.

Allowable Subject Matter

19. Claims 28/26, 30/29, 31-34 and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson D. Hernandez whose telephone number is (703) 305-8717. The examiner can normally be reached on 8:30 A.M. to 6:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R. Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nelson D. Hernandez
Examiner
Art Unit 2612

NDHH
Sept 2, 2004

NGOC-YEN VU
PRIMARY EXAMINER